PLEASE AMEND THE SPECIFICATION AS FOLLOWS:

After the title, insert -- This is a division of Patent Application serial number 10/056,622, filing date 1/28/02, now Patent No. 6,657,240 A Gate-Controlled, Negative Resistance Diode Device Using Band-To-Band Tunneling, assigned to the same assignee as the present invention.

REMARKS

A reference to the parent case has been added by Preliminary Amendment to this Divisional Patent Application.

The application is believed to be in condition for allowance. Allowance of the subject Patent Application is therefore respectfully requested.

Respectfully submitted,

STEPHEN B. ACKERMAN, REG. NO. 37,761

REMARKS

This is a full and timely response to the outstanding Action mailed June 3, 2004. Upon entry of the amendments in this response, claims 24 - 34 remain pending. In particular, Applicant has amended claims 24 and 29, has added claims 33 and 34, and has canceled claims 1 - 23 without prejudice, waiver, or disclaimer. Applicant has canceled claims 1 - 23 merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicant reserves the right to pursue the subject matter of these canceled claims in a continuing application, if Applicant so chooses, and does not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Indication of Allowable Subject Matter

The Office Action indicates that claim 25 would be allowed if rewritten in independent form including all of the limitations of its base claim. As set forth in detail below, however, Applicant respectfully asserts that independent claim 24, which serves as the base claim for claim 25, is in condition for allowance. Thus, Applicant respectfully asserts that claim 25 also is in condition for allowance as presented.

Claim objections

The Office Action indicates that claims 1 and 29 stand objected to because of various informalities. As best understood by Applicant, the pending objection has been lodged against claims 24 and 29 as claim 1 was previously canceled. As set forth above, Applicant has amended claims 24 and 29 and respectfully asserts that the rejection has been rendered moot.

Rejections under 35 U.S.C. 103

The Office Action indicates that claims 24, 26-28, and 31-32 stand rejected under 35 U.S.C 103(a) as being unpantentable over *Ebina* (U.S. 6,734,500) in view of *Finney* (U.S. 6,400,037). Additionally, the Office Action indicates that claims 29 and 30 stand rejected under 35 U.S.C 103(a) as being unpatentable over *Ebina* in view of *Finney* and further in view of Fig.1 Prior Art. Applicant respectfully traverses the rejection.

With respect to the cited references, Applicant respectfully asserts that both *Ebina* and *Finney* relate to bipolar junction transistor (BJT) devices, instead of the BBT transit diode devices recited in Applicant's claims. As known to one skilled in the art, a BJT device and a BBT transit diode device are two distinct devices that operate in different ways. For example, a BBT transit diode device is a two-terminal device formed of a p-n junction or an n-p junction and operated by applying voltages to the two terminals. A BJT device, however, is a three-terminal device formed of a p-n-p junction or an n-p-n junction, and operated by applying voltages to the three terminals. Accordingly, Applicant that it is improper to apply the teachings of either *Ebina* or *Finney* for the purpose of rejecting the present claims.

Furthermore, it is known that the emitter region and the collector region of a BJT device are formed by the same doped type, such as both n-type or p-type. In contrast, the emitter region

and the collector region of a BBT transit diode device are formed by the different doped types, such as one n-type and one p-type. Thus, these structures and functionality exhibited by these structures are quite different. Therefore, Applicant respectfully asserts that it is improper to attribute the emitter/base/body/collector structure of a BJT device to the emitter/barrier/drift/collector structure of a BBT transit diode device as claimed.

Additionally, Applicant respectfully asserts that even if either *Ebina* or *Finney* can be properly applied for the purpose of attempting to reject the present claims, it is improper to combine these references. Specifically, Applicant respectfully asserts that such a combination would be inoperative and/or the references teach away from such a combination. For example, the Office Action indicates that one would form a gate overlying a part of the emitter region, as taught by *Finney*, in *Ebina's* process to form an inversion channel and to improve reverse bias conducting properties of the device. Applicant respectfully disagrees with this contention. In particular, according to Col.2 lines 5-10 and 24-30 of *Finney*, the gate electrode 11 is extended across a part of the emitter region 6 for forming an inversion channel 13 to connect the further region 8 and the base region 4 across the emitter region 6 and allow current flow therebetween. Therefore, Applicant respectfully asserts that it is unreasonable to combine *Finney* with *Ebina* because there is no "region 8" in *Ebina's* structure, and an inversion channel cannot be formed even if Finney and Ebina are combined.

Moreover, as will be described in detail below, even if Ebina and Finney are combined, the combination fails to teach or reasonably suggest all the features/limitations recited in the pending claims.

By way of example, claim 24 recites:

> Claim 24 A method to form ***a gate-controlled, BBT transit diode device*** in the manufacture of an integrated circuit device comprising:
>
> providing a semiconductor layer in a substrate;
>
> implanting ions into said semiconductor layer to form an emitter region;
>
> implanting ions into said semiconductor layer to form a barrier region;
>
> forming an insulator layer overlying said semiconductor layer;
>
> ***patterning said conductor layer to form a gate wherein said gate overlies said barrier region and at least a part of said emitter region; and***
>
> ***thereafter implanting ions into said semiconductor layer to form a collector region and to complete said diode device in the manufacture of said integrated circuit device wherein a drift region is formed in said semiconductor layer where said gate overlies said semiconductor between said collector region and said barrier region.***

(Emphasis Added).

Applicant respectfully asserts that the cited references are legally deficient for the purpose of rendering claim 24 unpatentable because at least the features/limitations emphasized above are not taught or reasonably suggested by the references, either individually or in combination. Therefore, Applicant respectfully asserts that claim 24 is in condition for allowance. Since claims 25 – 32 are dependent claims that incorporate all the features/limitations of claim 24, Applicant respectfully asserts that these claims also are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

Newly Added Claims

Upon entry of the amendments in this response, Applicant has added new claims 33 and 34. Applicant respectfully asserts that these claims are in condition for allowance and that no new matter has been added. Specifically, claim 33 recites:

> Claim 33 ***A method to form a gate-controlled, BBT transit diode device*** in the manufacture of an integrated circuit device comprising:
>
> providing a semiconductor layer in a substrate;
>
> ***forming an emitter region and a barrier region in said semiconductor layer by implanting ions into said semiconductor layer with a common masking layer and performing a common annealing process***;
>
> forming an insulator layer overlying said semiconductor layer;
>
> ***patterning said conductor layer to form a gate wherein said gate overlies said barrier region and at least a part of said emitter region; and***
>
> ***thereafter implanting ions into said semiconductor layer to form a collector region and to complete said diode device in the manufacture of said integrated circuit device wherein a drift region is formed in said semiconductor layer where said gate overlies said semiconductor between said collector region and said barrier region.***

(Emphasis Added).

Applicant respectfully asserts that the cited references are legally deficient for the purpose of rendering claim 33 unpatentable because at least the features/limitations emphasized above are not taught or reasonably suggested by the references, either individually or in combination. Therefore, Applicant respectfully asserts that claim 33 is in condition for allowance. Since claim 34 is a dependent claim that incorporates all the features/limitations of claim 33, Applicant respectfully asserts that this claim also is in condition for allowance. Additionally, this claim recites other features/limitations that can serve as an independent basis for patentability.

Cited Art Made of Record

The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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